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## Stress evolution mechanism and thermo-mechanical reliability analysis of copper-filled TSV interposer

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### Highlights

- The stress evolution mechanism of TSV under thermal cycling was confirmed first time.
- The relationship between the stresses state and failures of TSV interposer was found.
- An original combined use of FEM simulation and failure analysis was proposed for TSV.

### Abstract

Through silicon via (TSV) has become one of the key emerging trends of three-dimensional (3D) packages, as it can realize vertically interconnect between stacked-dies. Due to large mismatch in thermal expansion coefficients (CTE) between the copper via and the silicon, significant mechanical stresses are induced at the interfaces when TSV structure is subjected to thermal stresses, which would greatly affect the reliability and electrical performance of TSV 3D device. In this paper, the relationship between the state of stresses and failure of TSV had been explored by combining finite element model simulation (FEM) and failure physical analysis. The position of the maximum stress of the TSV structure was obtained by FEM analysis. The relationship of stress and displacement change with temperature was also studied. And a thermal cycling experiment was conducted to validate the simulation results. Physical failure analysis after thermal cycling experiment was used to verify the degradation mechanism predicted by thermo-mechanical simulation.

### Keywords

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Through silicon vias, thermo-mechanical reliability, failure mechanism, finite element analysis, 3D integrated packaging, thermal cycling experiment.

### Acronyms and Abbreviations

TSV	Through silicon vias
FEM	Finite element modeling
SEM	Scan electron microscopy
TEM	Transmission electron microscopy
FIB	Focused ion beam
TC	Thermal cycling
CTE	Thermal expansion coefficients

### Notations

(C)	Specific heat capacity matrix
(K)	Heat conduction matrix
{T}	Heat storage term
Q(t)	Heat energy

### 1. Introduction

With the development of three-dimensional (3D) integrated packaging [3, 5], Through Silicon Via (TSV) has become one of the most promising technologies in realizing 3D stacking package [1, 21]. Advanced TSV technology can realize 3D heterogeneous integration [28], high speed, wide band, small size and high performance through vias and micro-bumps. TSV is an important physical and electrical connection between chips [19], and the reliability of TSVs affects considerably on the reliability of 3D integrated devices [18]. However, TSV technology faces many difficulties and challenges in processing [12, 16]. Moreover, its reliability has not been fully understood [15]. Thus it is of paramount significance to investigate stress evolution mechanism and thermo-mechanical reliability of copper-filled TSV.

The thermo mechanical reliability of the TSV structure is one of the most concerned research fields at present [30]. In the typical TSV manufacturing process, copper is often used as the conductive material to fill the TSVs [14]. The mismatch between copper and silicon's thermal expansion coefficient (CTE) is significant [11]. To be specific, under the condition of rapid temperature change, the expansion rate

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of the copper column is much greater than the silicon body. Therefore, the interface between the copper column and the silicon body will generate huge stress [7], which eventually causes failures of TSVs like silicon crack, delamination between the interface of the copper column and the silicon body, etc. [20].

The study on thermo-mechanical reliability of TSV structure mainly focuses on two aspects: Stress Simulation [27] and thermal cycling experiment [11]. Feng [13] investigated the radial and axial thermal stresses of a novel TSV structure using polarized Raman spectroscopy and a finite element simulation. Pan [26] established a numerical model of Cu-filled TSV to simulate and analyze the effect of diameter, aspect ratio (AR) and defects on TSV thermal stress and deformation. The effects on the material properties of the underfill layer on thermal stress and deformation in 3D TSV integration packages were evaluated through numerical analysis in Ref. [32]. However, the stress evolution mechanism has not been verified by experiments on real 3D TSV integration packages in above literatures. Many researchers have attempted to reveal the degradation mechanism of TSV structure under thermal stresses by employing failure analysis[2, 6]. The barrier and dielectric liner degradation in a copper (Cu) TSV structure are evaluated via a non-destructive electrical characterization method after different stress tests such as high temperature storage, temperature cycling and electrical biasing, see Ref. [8]. The reliability TSV daisy chains under thermal cycling conditions was examined in Ref. [10]. However, there are rare systematic literature devoted to verifying the relationship between the state of stress and TSV failures by combining simulation with failure physical analysis. Hence, in this paper, we explore the relationship between the state of stresses and failures of copper-filled TSV interposer. Moreover, the stress evolution mechanism has also been verified.

This paper is organized as follows: Section 2 describes the thermo-mechanical stress simulation analysis result of typical TSV interposer under thermal cycling stress. Section 3 demonstrates the observed failure modes of the actual sample after thermal cycling experiment. Section 4 analyzes the stress evolution mechanism by microscopic physical analysis at nanometer scale. Discussions are given in Section 5 and finally a conclusion is wrapped up in Section 6.

## 2. Thermo-mechanical Stress Simulation Analysis

### 2.1. Sample Introduction

The sample is a silicon interposer with a 100µm deep and 10µm long copper-filled TSV which has a 50nm thick Ti barrier and 250nm thick SiO<sub>2</sub> dielectric layer. The TSV connects two metal levels of damascene redistribution copper at the top with one metal level of damascene redistribution copper at the bottom. The surface dielectric layer silicon interposer is polyimide. The sectional structure of the TSV silicon interposer is shown in Fig. 1.

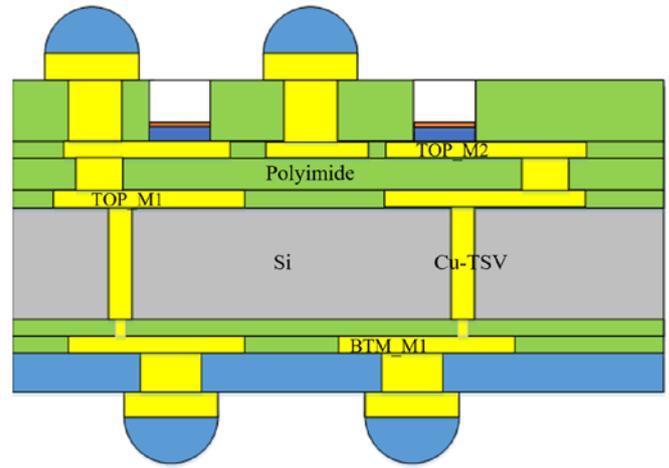


Fig. 1. The sectional structure of TSV silicon interposer.

### 2.2. Finite Element Model

To study the correlation between stress distribution by thermal cycling and failures, the finite element analysis software ANSYS [9] is employed to implement simulation analysis [4]. The APDL which is parametric design language of ANSYS is used to establish a solid model of the TSV structure and mesh it. The numerical simulation of the TSV thermal cycling test is a transient thermal-structural coupling simulation, which includes interacting coupled physical fields (thermal and structural fields) and has a large deformation. In order to ensure the accuracy of the calculation and speed up the calculation convergence time, in the thermal-structure coupling analysis, the direct coupling analysis method is used. PLANE 13 of the two-dimensional coupled field solid element is used to calculate the element matrix or element load vectors containing the thermal field and the stress field for coupling. PLANE 13 has 4 nodes, each node has 4 degrees of freedom and has large deformation and stress stiffness capabilities. It can realize the large deformation coupling between the thermal field and the structural field. It is solved by setting the element real constant to the plane stress.

During the thermal cycling process, the temperature field distribution is a function of temperature and time. From Fourier's law, it can be known that the heat flux of an object is related to the rate of temperature change. The TSV interposer is placed in a variable thermostat, which only considers heat conduction and heat convection, and ignores the effects of heat radiation. The thermal cycling condition is shown in Fig. 3. The temperature cycle stress condition is a function of temperature and time. The temperature range is from -55°C +125°C. The conversion between high temperature and low temperature is completed within 60s. The retention time of high temperature and low temperature is also 14 minutes. In order to express the temperature load that changes with time, the load-time curve (0-1800s load diagram) is divided into load steps, that is, each inflection point

Table 1. Material parameters

Material	Si	TSV-Cu	SiO <sub>2</sub>	Ti	PI
Young's modulus (GPa)	131	120	72	116	0.15
CTE (ppm/°C)	2.8	17.7	0.55	8.6	25
Poisson's ratio	0.3	0.36	0.16	0.32	0.37
Heat conductivity coefficient (kg*m/s <sup>2</sup> °C)	150	401	7.6	21.9	0.35
Specific heat capacity (m <sup>2</sup> /s <sup>2</sup> °C)	168	420	966	520	1100
Density (kg/m <sup>3</sup> )	2.35*10 <sup>3</sup>	8.4*10 <sup>3</sup>	2.2*10 <sup>3</sup>	4.5*10 <sup>3</sup>	1.43*10 <sup>3</sup>

in the load-time curve is a load step. For each load step, the corresponding load value and time value are defined, and the step or gradient load is set. In addition to the elastic modulus, Poisson's ratio, and thermal conductivity coefficient of the material, density and specific heat capacity is also needed in transient analysis. The governing equation for transient thermal analysis is as follows:

$$(C)\{T\} + (K)\{T\} = \{Q(t)\} \quad (1)$$

Where (C) is the specific heat capacity matrix, (K) is the heat conduction matrix, {T} is the heat storage term, and Q(t) is the heat energy. Uneven temperature distribution can cause thermal stress on components. TSV interposer is composed of multiple materials, and the thermal expansion coefficients of the different materials differ greatly, which can easily cause thermal mismatch.

Simulation material parameters are listed in Table 1. Elastoplastic

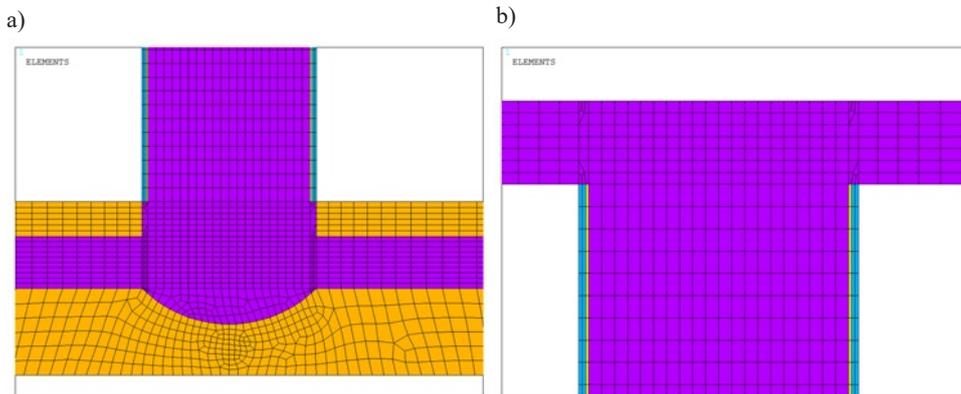


Fig. 2. Local mesh generation (a) the top (b) the bottom.

models [29] are used for Cu and Ti, and linear elastic models are used for SiO<sub>2</sub> and Si. Reference temperature without stress is 25°C. Axisymmetric two-dimensional structure model and local mesh generation are shown in Fig. 2. Note the mesh could not be generated due to the big difference of the structure size between Ti and other materials, hence  $\mu\text{m/kg/s}^\circ\text{C}$  as units and appropriate size tolerance are used in the calculation. To facilitate convergence, force control standards are used in the process of calculation.

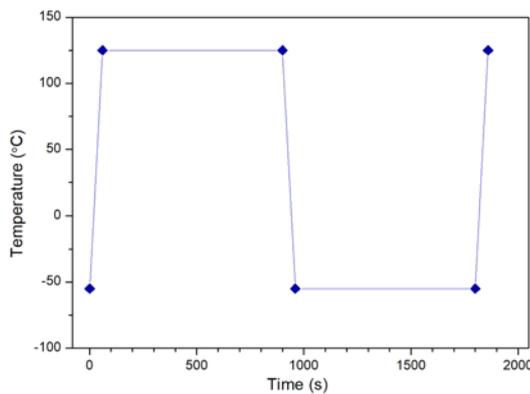


Fig. 3. Thermal cycling condition.

### 2.3. Simulation Results

The Mises stress distribution cloud diagram of the TSV interposer indicates that under thermal stress, uneven stress and strain appear in the TSV structure, which is analyzed by the elastoplastic yield cri-

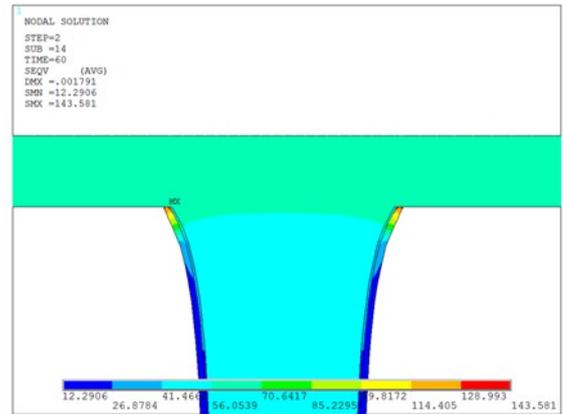


Fig. 4. Absolute maximum stress values point by FEM analysis.

terion [23]. As shown in Fig. 4, it shows that the maximum stress value of the TSV structure locates at the corner of the interface between Top\_M1 and TSV when subjected to thermal stress. On the Cu/Ti/SiO<sub>2</sub> interface where the thermal stress distribution is not uniform, the stress is gradient descending from the TSV interface to the central area.

As temperature rises from negative to positive, the mises stress maximum values gradually increase. As shown in Fig. 5, the mises stress maximum value is 47.84MPa at 20 seconds, then goes up to 143.58MPa at 60 seconds, as shown in Fig. 6. The mises stress maximum value is constant

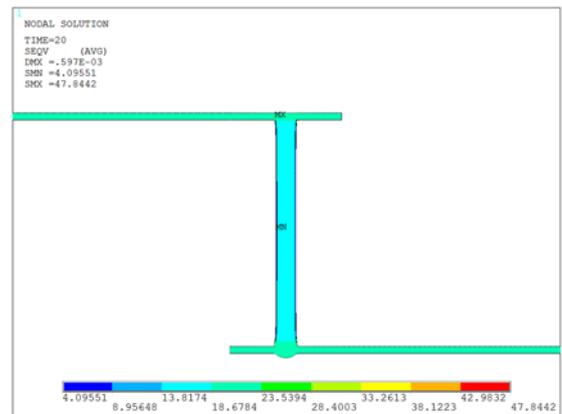


Fig. 5. Mises stress distribution cloud diagram at 20 seconds

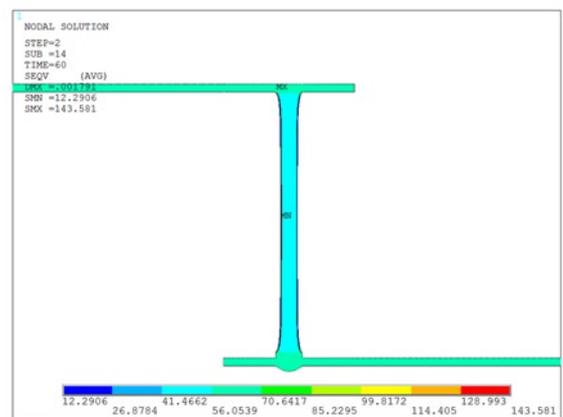


Fig. 6. Mises stress distribution cloud diagram at 60 seconds

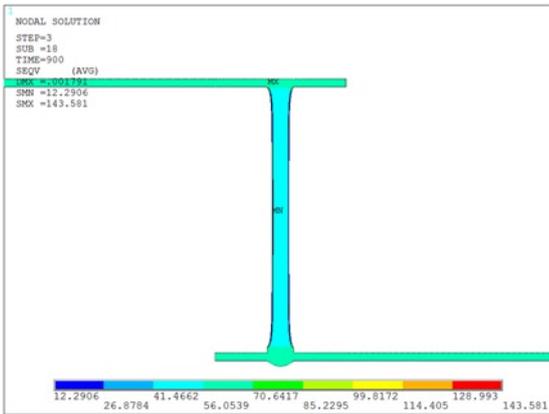


Fig. 7. Mises stress distribution cloud diagram at 900 seconds

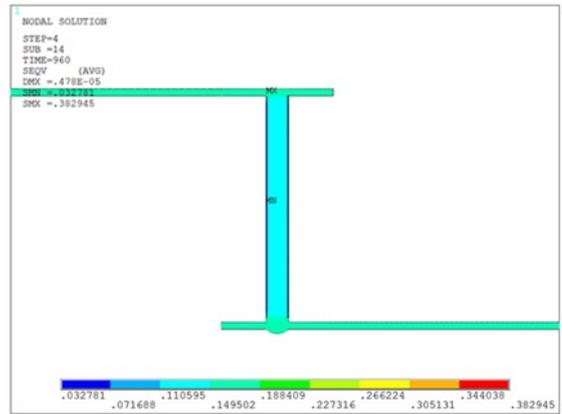


Fig. 8. Mises stress distribution cloud diagram at 960 seconds

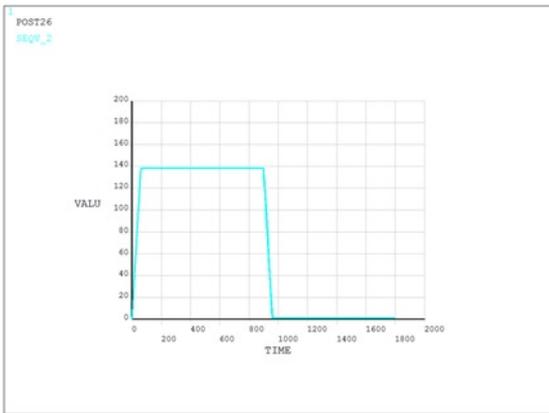


Fig. 9. A cycle period curve of mises stress value at a certain point

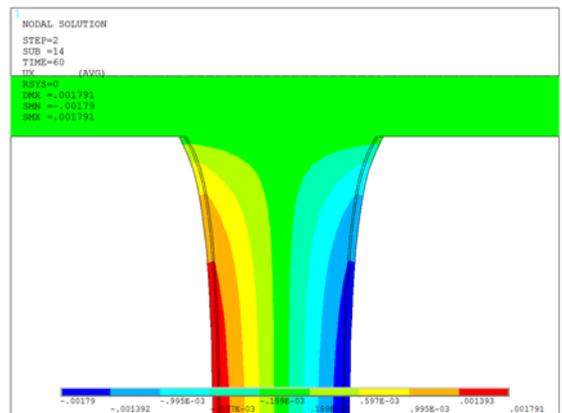


Fig. 10. The total displacement in the X direction at 60 seconds

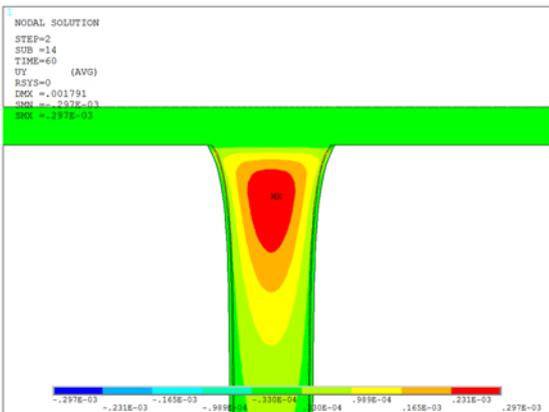


Fig. 11. The total displacement in the Y direction at 60 seconds (upper ends)

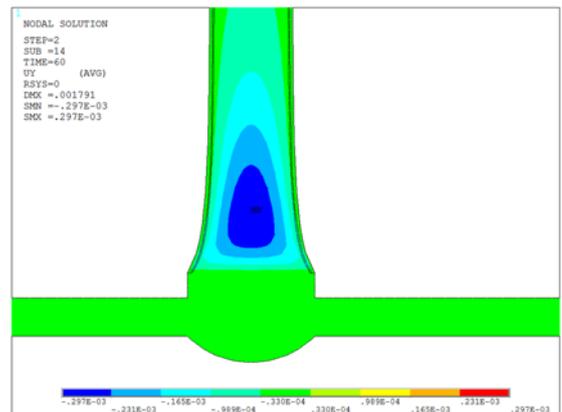


Fig. 12. The total displacement in the Y direction at 60 seconds (lower ends)

during temperature maintenance period. At 900 seconds, the mises stress maximum value is 143.58MPa, hardly changes than the value at 60 seconds, as shown in Fig. 7. As the temperature drops from positive to negative, the mises stress maximum value gradually decreases. At 960 seconds, the mises stress maximum value was 0.38MPa, which is approximately equal to the initial stress value, as shown in Fig. 8. A cycle period curve of mises stress value at certain stress concentration points as shown in Fig. 9 also demonstrates the trend of stress change with temperature.

From displacement simulation results, as temperatures rising, in the X-direction both sides of TSV displaced towards the middle and the maximum displacement value appeared at the center of both sides. As shown in Fig. 10, the maximum displacement at the center of the left side of TSV is  $1.791 \cdot 10^{-3}$  um, and the right is  $-1.791 \cdot 10^{-3}$  um. In the Y direction, both ends of the TSV show an obvious tensile trend.

As shown in Fig. 11, the maximum displacement at the upper end of TSV was  $0.297 \cdot 10^{-3}$  um, and the lower end was  $-0.297 \cdot 10^{-3}$  um.

As the temperature rises from negative to positive, the displacement gradually increases. The maximum displacement value in the X direction at 20 seconds and 60 seconds is  $0.597 \cdot 10^{-3}$  um and  $1.791 \cdot 10^{-3}$  um respectively (Fig. 13&14). The maximum displacement value remains unchanged during the temperature maintenance period, and at 900 seconds, the maximum displacement value is  $1.791 \cdot 10^{-3}$  um, as shown in Fig. 15. As the temperature decreases from positive to negative, the maximum displacement value gradually decreases. At 960 seconds, the maximum displacement value was  $0.478 \cdot 10^{-5}$  um, which was approximately equal to the initial displacement, as shown in Fig. 16.

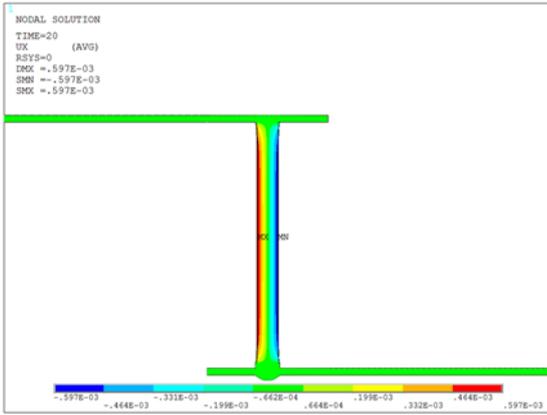


Fig. 13. The total displacement in the X direction at 20 seconds

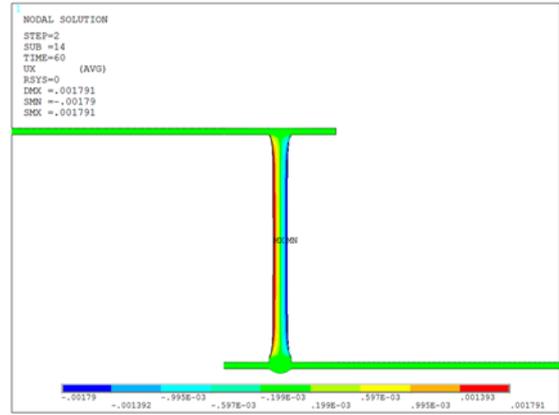


Fig. 14. The total displacement in the X direction at 60 seconds

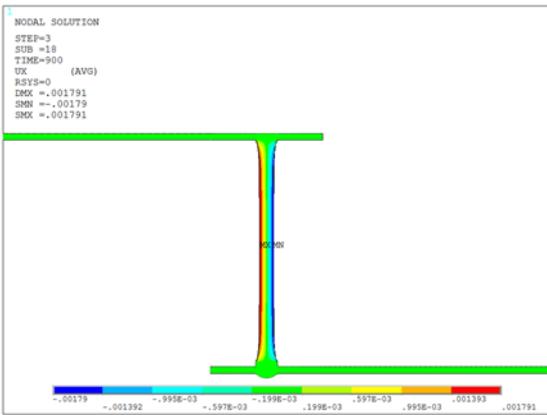


Fig. 15. The total displacement in the X direction at 900 seconds

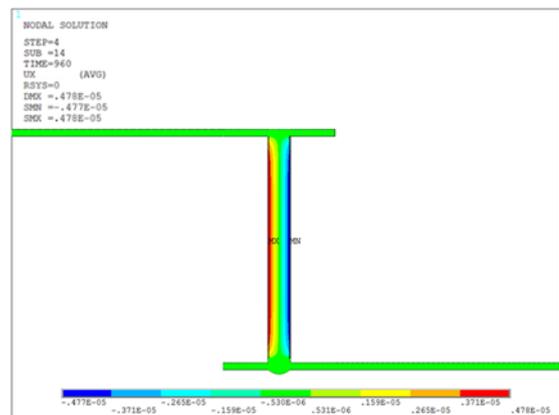


Fig. 16. The total displacement in the X direction at 960 seconds

### 3. Thermal Cycling Experiment

To verify the correlation between simulation results and failure mode, thermal cycle experiments [17, 25] were carried out, and the experimental conditions were consistent with the temperature load condition adopted in the simulation.

The test structure for the thermal cycling experiment includes 13 groups of TSV daisy chains [16], and each group of daisy chains includes 8 groups of TSVs. After 1000 thermal cycles, a statistical analysis of the DC electrical resistance as a function of thermal cycling is obtained and presented in Fig. 17. It is observed that the resistance of the TSV daisy chain of No.1, 2, 6, and 13 increased significantly with the number of thermal cycles.

Cross-section analysis [22] of the TSV daisy chain of No.1 had been carried out, and the following failure modes were observed at the interface between Top\_M1 and TSV, as shown in Fig. 18:

- 1) Copper-Filled TSV was deformed from the uniform thickness to a “U-shape” thickness, as shown in Fig. 19.
- 2) Deformation occurred at the connection between TSV and BTM\_M1, as shown in Fig. 20.
- 3) Voids appeared in filled copper, as shown in Fig. 21.

### 4. Degradation Mechanism Analysis

To further analyze the failure mechanism [24, 31] of TSV samples after thermal cycling experiment, TEM analysis was performed. Firstly, a dual-beam focused ion beam (FIB)-SEM tool (Zeiss Auriga Compact) was used to slice parallel to the cross-sectioned surface. The top view of TSV for FIB preparation was shown in Fig. 22. To extract the slices at failure site, a trench was dug with 5 μm depth, 7 μm long, and 8 μm wide, as shown in Fig. 22(b). The FIB cross-section appearance at the interface between Top\_M1 and TSV was shown in Fig. 23, and from this cross-section appearance it could be judged whether the dug depth is appropriate or not. Before slices extraction, the thickness of the slices should be no less than 1 μm. The slices were extracted by the manipulator and placed on the copper net. To meet the requirements of TEM analysis, the slices should be thinned to about 100nm. The slice for TEM analysis at the interface between Top\_M1 and TSV is shown in Fig. 24.

Then, the prepared slice was observed by the transmission electron microscope (TEM) model JEM-2100F with 0.25nm point resolution, 0.102nm line resolution and 0.20nm STEM resolution. According to the STEM appearance as shown in Fig. 25 and the TEM appearance as shown in Fig. 26, it is confirmed that under thermal cycling stress, the crack first appears at the corner of the interface between Top\_M1 and TSV with the maximum stress value (as shown by the arrow), and then extended towards the inside of TSV. This agrees with the simulation results.

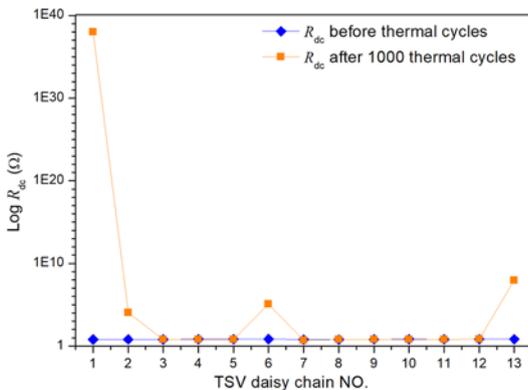


Fig. 17. The DC electrical resistance change (the logarithmic coordinate)

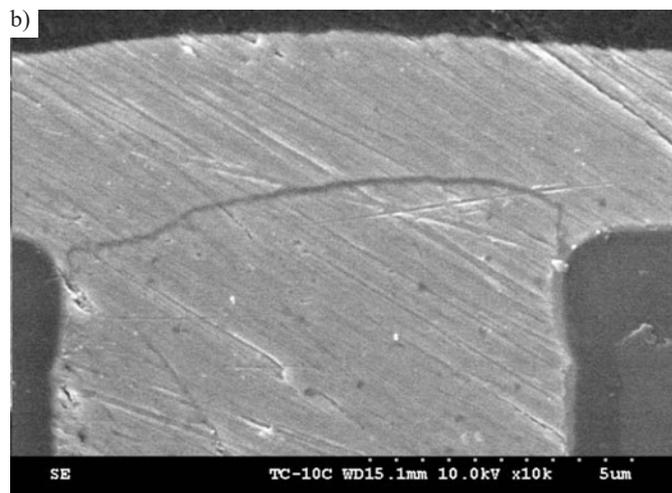
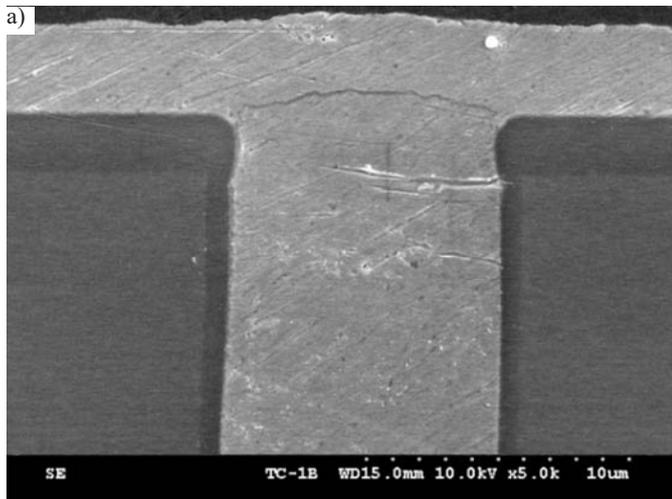


Fig. 18. Cracks at the interface between Top\_M1 and TSV (a) failure TSV 1 (b) failure TSV 2

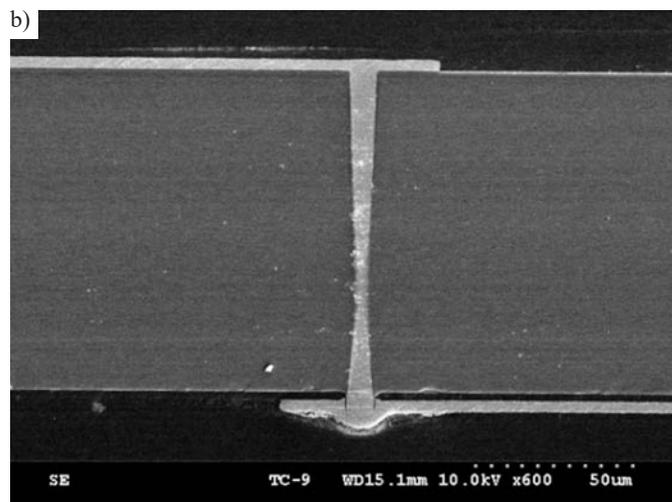
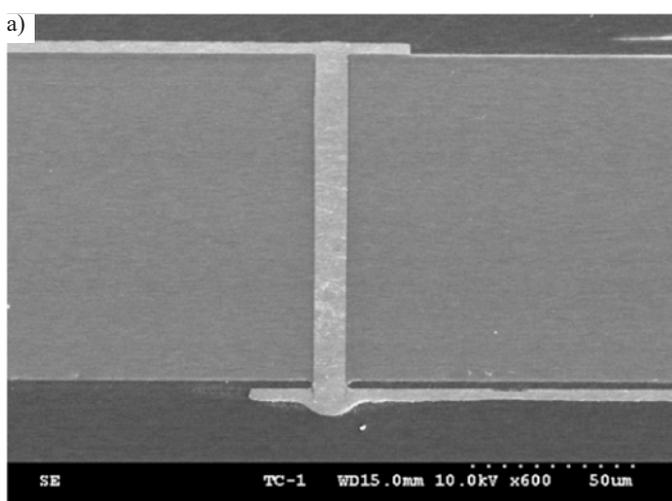


Fig. 19. Copper-Filled TSV deformation from uniform thickness to thin in the middle and thick at the ends (a) normal appearance (b) failure appearance

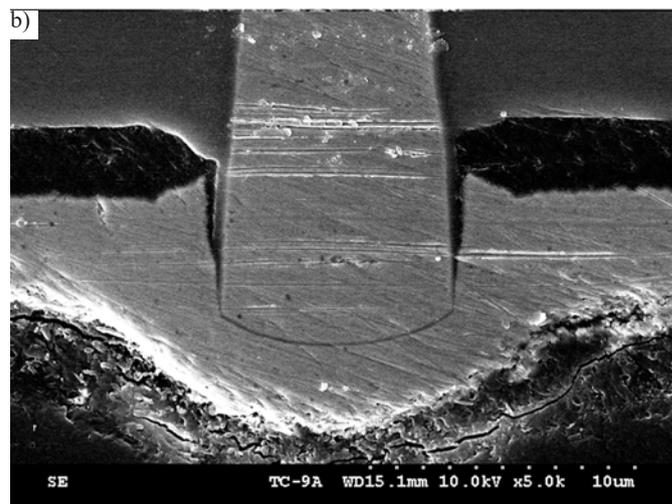
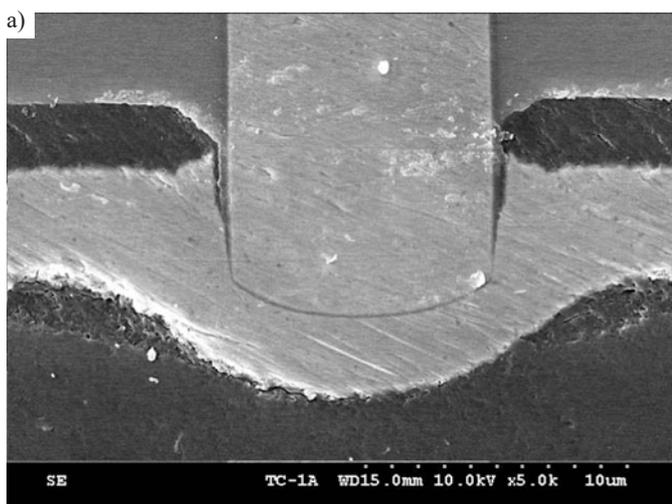


Fig. 20. Deformation at the connection between TSV and BTM\_M1 (a) normal appearance (b) failure appearance

Besides, the distribution and diffusion behavior of elements at the interface had also been investigated by Bruker XFlash 5030T X-ray energy spectrometer equipped with silicon drift detector (SDD) with energy resolution better than 123eV within the input count rate of 100,000cps which provided an important clue to confirm the failure mechanism. As shown in Fig.27 and Fig.28, the TSV interface had

four elements: Si, O, Ti, and Cu, which is corresponding with four interface materials. From the distribution of the Ti element, after crack took place at the corner of the interface between Top\_M1 and TSV with the maximum stress value, the Ti elements spread along the crack towards the Cu substrate. The diffusion behavior of the Ti element had

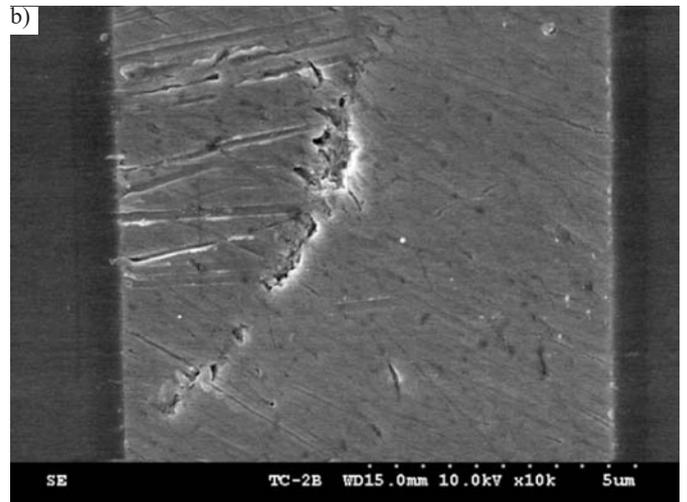
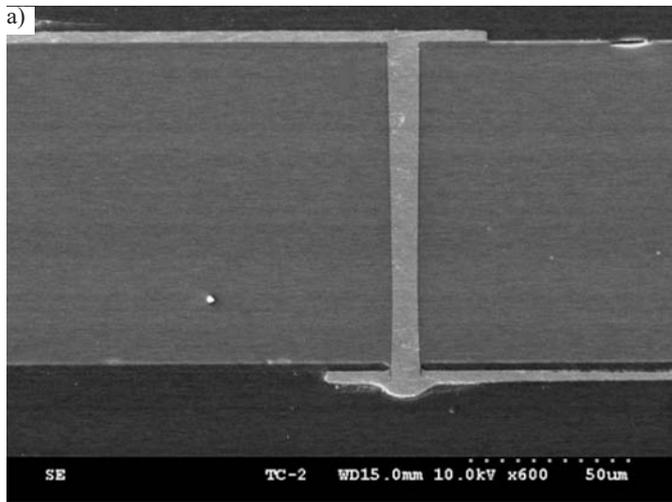


Fig. 21. TSV void (a) failure site (b) local magnification appearance

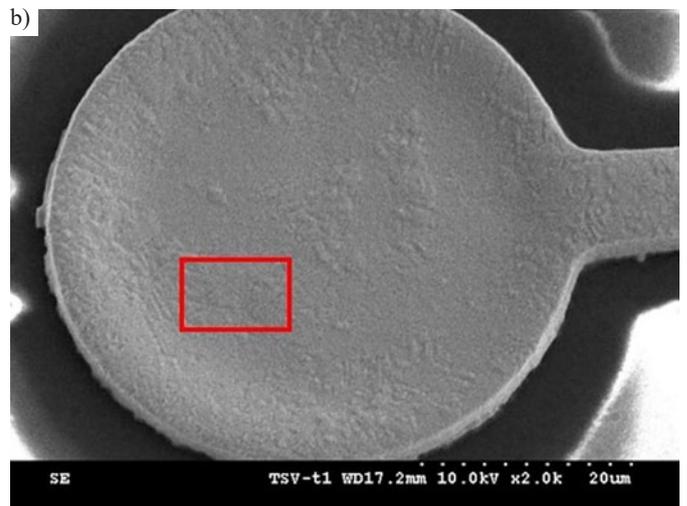
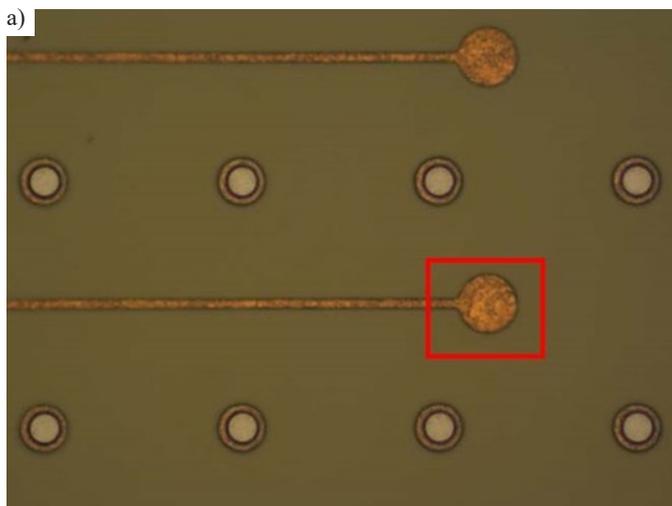


Fig. 22. The top view of TSV for FIB preparation (a) Metallographic microscope appearance (b) SEM appearance

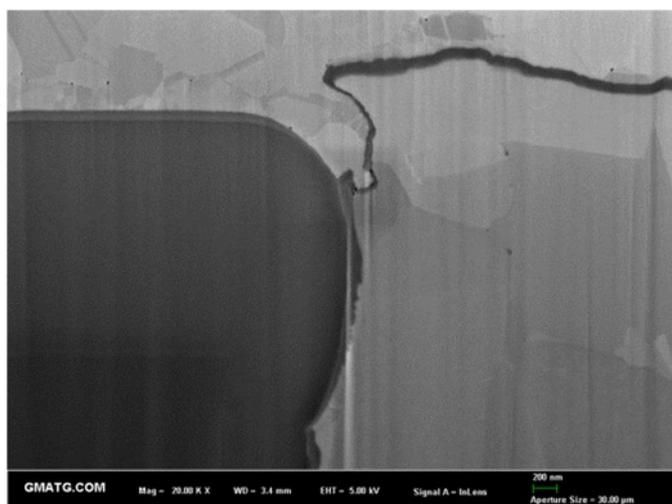


Fig. 23. FIB cross-section appearance at the interface between Top\_M1 and TSV

a good corresponding relationship with the physical mechanism of crack initiation and propagation.

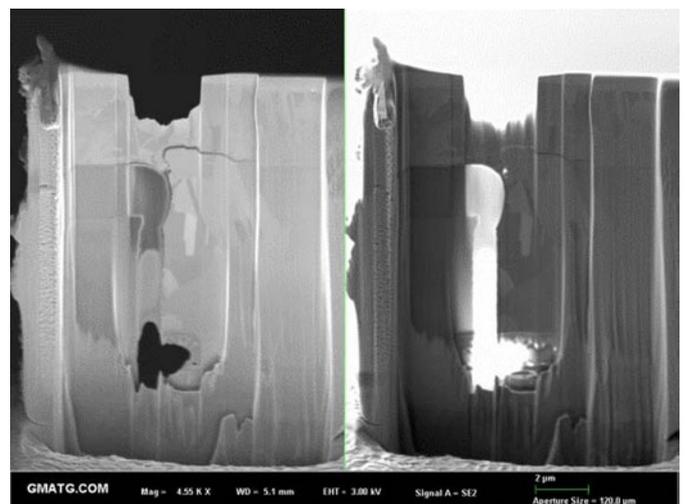


Fig. 24. Slice for TEM analysis at the interface between Top\_M1 and TSV

## 5. Discussion

Mises stress distribution cloud diagram showed that the maximum stress value of the TSV appears at the corner of the interface between Top\_M1 and TSV under thermal stress. This is because of the serious thermal mismatch caused from the thermal expansion coefficient dif-

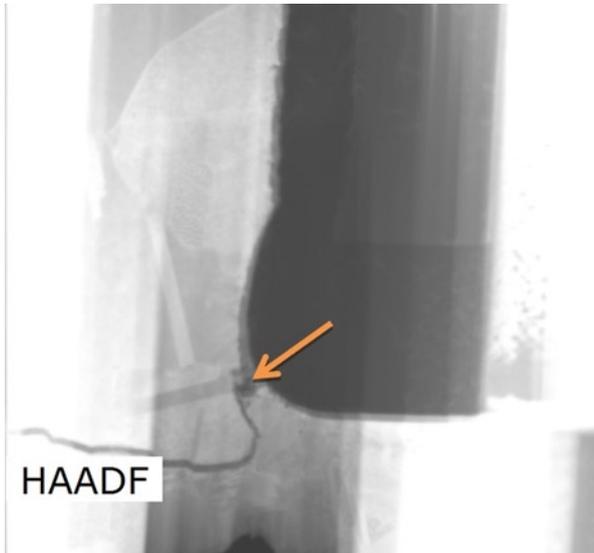


Fig. 25. STEM appearance at the interface between Top\_M1 and TSV

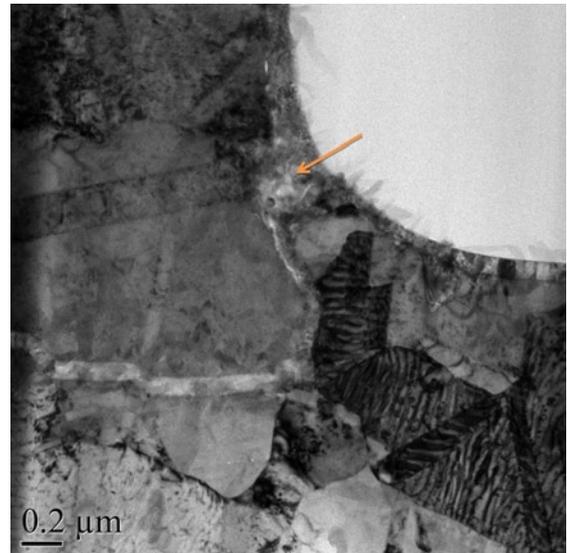


Fig. 26. TEM appearance at the interface between Top\_M1 and TSV

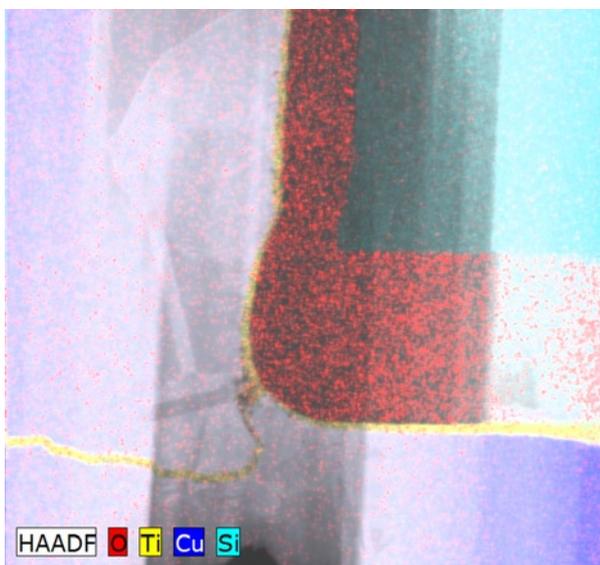


Fig. 27. Element analysis of TSV interface (four elements) overlay

ference of copper and silicon dioxide (two orders of magnitude). Besides, it is easier to produce stress concentration around the corner.

As temperature increases, the mises stress and displacement values gradually increase. This is related to the thermal properties of materials.

The crack areas observed after the actual thermal cycling experiment is in a good corresponding relation with stress concentration areas simulated by finite element analysis. Under thermal cycling stress, first, the crack appears at the corner of the interface between Top\_M1 and TSV with the maximum stress value, and then it extends toward the inside of TSV. As a result, crack is observed at the interface between Top\_M1 and TSV by scanning electron microscopy (SEM).

TSV deformations after the actual thermal cycling experiment also have a good corresponding relation with displacement simulation results. From displacement simulation results, as temperatures rise, in X-direction both sides of TSV displaced toward the middle and the maximum displacement value appears at the center of both sides. In Y direction, both ends of the TSV shows an obvious tensile trend. By

SEM, it is found that the copper-filled TSV deformation from uniform thickness to thin in the middle and thick at the ends under the action of thermal cycling stress. The upper and lower ends show obvious tensile deformation. The left and right sides extrude toward the middle. The axial stretching of the metal accumulates at both ends of TSV, which results in deformation at the connection between TSV and BTM\_M1.

Voids that appeared in filled copper are related to electromigration under thermal stress. TEM appearance and diffusion behavior of Ti element confirm the physical mechanism of crack initiation and propagation.

## 6. Conclusions

In this paper, the relationship between the state of stresses and failure of TSV has been explored. FEM-based thermo-mechanical analyzes are performed to understand stress distribution and change in the TSV interposer. Subsequently, a thermal cycling experiment is performed to verify the simulation results. Based on FIB-SEM analyses, four different damage types are observed in the TSV interposer; TSV-M1 interface cracks, TSV voids, TSV-bottom deformation, and TSV “U-shape” deformation. TSV deformations after the actual thermal cycling experiment have a good corresponding relation with displacement simulation results. Voids that appeared in TSV are related to electromigration under thermal stress. Combining FEM simulation analysis and TEM physical analysis, it is found that the crack site is correlated with the distribution of stress in the TSV interposer, the crack first appears at the corner of the interface between Top\_M1 and TSV with the maximum stress value, and then extended towards the inside of TSV.

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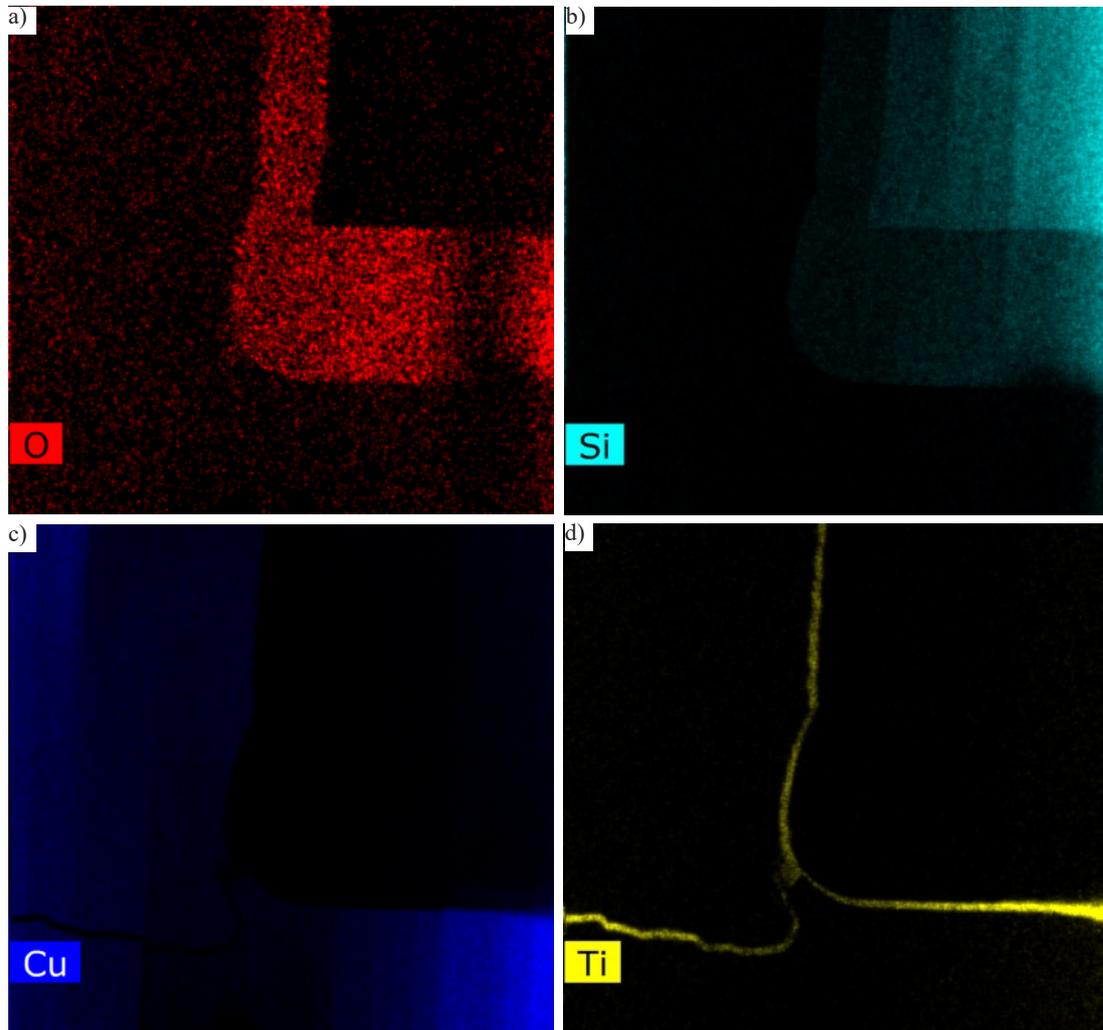


Fig. 28. Element analysis of TSV interface (each element) (a) O element (b) Si element (c) Cu element (d) Ti element

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